FORM LD-1

APPLICATION FOR REGISTRATION OF LAYOUT-DESIGN

[Section 8(1), Rule 22]

(to be filed in triplicate)

Application is hereby made for the registration of layout-design[1] ——————in the name(s)[2] of ——————— whose address(s)[3] ——————is claim(s) to be the proprietor thereof in respect of the said layout-design.

Endorsed herewith is the duly completed Statement of Particulars relating to the layout-design

The particulars set forth in the enclosed Statement of Particulars are true to the best of my/our knowledge, information and belief.

Dated this ——————day of ——————20—.

[4]_____

To

The Registrar Semiconductor Integrated Circuits Layout-Design, Office of the Semiconductor Integrated Circuits Layout-Design Registry at[5] ————.

1. Title of the layout-design.
2. Insert legibly the full name, description and nationality of the applicant. In the case of a body corporate or firm the country of incorporation or the names and description of the partners composing the firm and the nature of registration, if any, as the case may be, should be stated. See rule 15.
3. The applicant must state the address of his principal place of business in India, if any. See rules 3 and 16.
4. Signature of the applicant or his agent (legal practitioner or registered layout-design agent or person in the sole and regular employment of the applicants. See section 84).
5. State the name of the place of the appropriate office of the Semiconductor Integrated Circuits Layout-Design Registry. See rule 4.
6. Layout-design drawings should be preferably on a paper of size 33-centimeter by 20-centimeter.

Statement of Particulars

(Refer Form LD-1)

1. Application No. (to be filled in by the Semiconductor Integrated Circuits Layout-Design Registry):
2. Title of the layout-design
3. Classification of the semiconductor integrated circuit which can be manufactured using the layout-design
   - (i) Structure[1]
   - (ii) Technique[2]
   - (iii) Function[3]
4. Brief description of the layout-design
5. Whether the layout-design has been commercially exploited [Yes /No]

   If yes, then in Place / Country ——————— on Dated this ——————day of ——————— Year —
6. Documents enclosed
   - (i) Drawings/ photograph (three sets)
   - (ii) Semiconductor integrated circuits (4 pieces)

     [Where an Integrated Circuit (IC) has been made using layout-design applied for registration]
   - (iii) Details of the fees deposited
   - (iv) Others
7. Name and address of the agent
8. Others, if any

Place: [4]_____

Date:

1. Structure implies giving structure details like Bipolar, MOS, Bi-MOS, Optical IC, Other (specify).
2. Technique implies giving technique details like TTL, DTL, CMOS, NMOS, PMOS, Other (specify).
3. Function implies giving functional details like Logic, Memory, Linear, Microcomputer, Other (specify)
4. Signature of the applicant or his agent (legal practitioner or registered layout-design agent or person in the sole and regular employment of the applicant. See section 84.)